A W-Band LNA Using Parallel Coupled Transmission Lines

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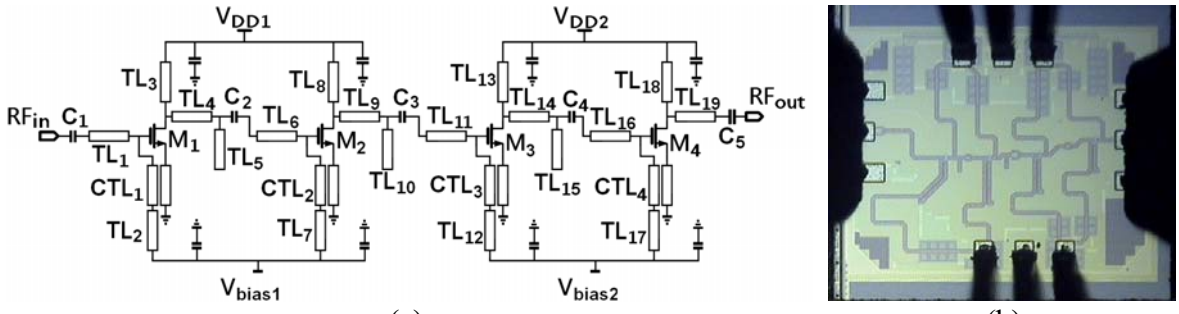
Abstract

A W-band low-noise amplifier (LNA) of four stages of common source topology is proposed in this paper. The chip was fabricated by using 90-nm CMOS process technology. It adopted parallel-coupled transmission lines between the gate terminal and the source terminal of the NMOS. Such structure was applied for optimizing among the noise, input matching and the gain. The measured results showed a peak gain of 13.15 dB at 73 GHz; a minimum noise figure of 4.83 dB at 77.5 GHz; an input P_{1dB} of –7.3 dBm at 78 GHz, and an IIP3 of –1.1 dBm. The chip area is 0.730×0.588 mm^2, and the total power consumption is 28.14 mW under 1.2-V supply.

1 Circuit Design

Low noise amplifier (LNA) is a key component in the RF/microwave front end. LNAs are often focused on gain, noise, power and linearity. These specifications are hard to reach simultaneously. Among the design techniques, simultaneous input power and noise matching is usually achieved by employing source degeneration technique [1], [2]. In the microwave range, it can be realized by using parallel coupled transmission lines. Proper designed parallel coupled transmission lines can arise the gain without degrading noise. By using transistors in parallel and flattened layout, it is able to optimize noise effectively. This proposed LNA adopted above-mentioned techniques in order to achieve excellent performance for noise, input matching, and linearity. The schematic of the proposed LNA is shown in Fig. 1(a) and the micrograph of the fabricated chip is shown in Fig. 1(b) with a size of 0.730×0.588 mm^2. The LNA is consisted of 4 common-source stages with inductive degeneration. All the required inductive components are realized by microstrip lines or parallel coupled transmission lines. In this design, the main concern of the first two stages is the noise performance and we adopted larger NMOS sizes and longer coupled lines. Whereas we chose smaller NMOS sizes and shorter coupled lines in the last two stages for the gain and bandwidth consideration.



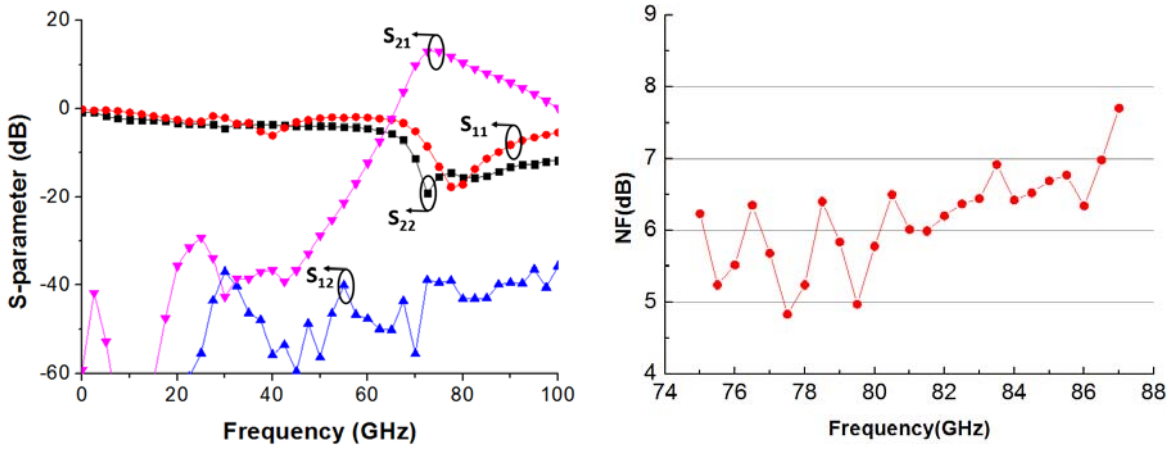
(a) (b)

Figure 1: The proposed W-band LNA: (a) schematic, and (b) micrograph.

2 Measured Results

We performed all the measurements by using on-wafer probing test. Under a 1.2 V supply voltage, the measured dc power consumption of this LNA is 28.14 mW. Fig. 2(a) shows the

measured results of S-parameters. It can be seen that the frequency ranges for $|S_{11}|$ and $|S_{22}|$ below –10 dB are from 73 to 86 GHz and from 70 to 100 GHz, respectively. The peak gain is 13.15 dB at 73 GHz with a smaller gain of 11.422 dB at 78GHz and –3-dB gain bandwidth range is from 71 to 80 GHz which meets the general 12 dB gain requirement. The reverse isolation is better than 32 dB in whole measured frequency range. Fig. 2(b) shows the measured noise figure (NF) of the proposed W-band LNA. The measurement range is from 75 to 87 GHz. The measured noise figure is 5.24 dB at 78 GHz, and the lowest point is 4.83 dB at 77.5 GHz. In the range from 75 to 86 GHz, the measured NF is below the level of requiered 7 dB. The measured input 1-dB compression point (P_{1dB}) and input third order intercept point (IIP3) of this proposed LNA at 78 GHz are –7.3 dBm and –1.1 dBm, respectively.



(a) (b)

Figure 2: The measured (a) S-parameters and (b) noise figure of the W-band LNA.

3 Conclusion

We have successfully implemented a W-band LNA in the 90-nm CMOS process. By using the technique of coupled transmission lines between the gate terminal and the inductive degenerative transmission line, we can simultaneously achieve input power matching and noise matching. This work shows a lowest NF of 4.83 dB, power gain of 11.42 dB, input P_{1dB} of –7.3 dBm and IIP3 of –1.1 dBm at 77-79 GHz range while consumes a 28.14 mW power from a 1.2-V supply. The LNA shows a better linearity and noise performance by using the proposed parallel coupled transmission lines compared with most previous published works.

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